

Claim rejections

Claims 1-3, 15 and 17 are rejected under 35 U.S.C. §102(b) as anticipated by Matsunaga et al. (U.S. 2001/0042141) ("Matsunaga"). Applicants respectfully traverse this rejection.

Matsunaga does not support the rejection for at least the reason that it fails to disclose "an address comparison section which reads out a second address and compares the stored first address and the read-out second address, the second address being stored in a page table element having the same element number as the page table element in which the first address is stored among page table elements of a page table specified by a second command packet, when the second command packet is transferred through the first bus after the bus reset occurs" as recited in claim 1.

One illustrative example of this feature is shown in FIG. 16 of the present application. As shown in FIG. 16, the page table before the bus reset includes the page table elements PE11 to PEM1, and the page table after the bus reset includes the page table elements PE12 to PEM2. The address ADK1 stored in the page table element of the page table before the bus reset and the address ADK2 stored in the page table element of the page table after the bus reset are compared. In this way, data transfer can be restarted from the page table element processed at the time of the bus reset.

By contrast, in Matsunaga, the content of the ORB1 before the bus reset and the content of the ORB2 after the bus reset are compared, as indicated by D4 in Fig. 11 of Matsunaga. This is different from comparing addresses stored in the page table elements of the page table as recited in claim 1, and there are associated disadvantages. Matsunaga's approach may cause a data transfer to be restarted when it is not appropriate to do so. For example, the addresses started in the page table specified by the ORB1 before the bus reset

may be AD1, AD2, AD2, AD4, etc., whereas the addresses specified by the ORB2 after the bus resent may be AD1, AD5, AD6, AD7, etc. In this case, the data transfer should not be restarted even if they share the same start address AD1. In view of this, the structures recited in claim 1 of the present application ensure a normal operation at the time of a bus reset in a more reliable manner than does Matsunaga's arrangement.

Accordingly, claim 1 is allowable over Matsunaga, as are claims 2, 3, 15 and 17 for at least the reason that they depend on claim 1. Withdrawal of the rejection is therefore respectfully requested.

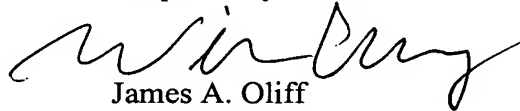
Claim 5 is rejected under 35 USC § 103(a) as being unpatentable over Matsunaga in view of Bastiani et al. (US 6,636,922). Claims 7 and 9 are rejected under 35 USC § 103(a) as being unpatentable over Matsunaga in view of Bastiani et al. and further in view of Ogawa (JP 01106254). Claims 11 and 13 are rejected under 35 USC § 103(a) as being unpatentable over Matsunaga in view of Bastiani et al. in view of Ogawa, and further in view of Graziano (US 5,758,075). Applicants respectfully traverse the rejections.

Each of the noted claims depends directly or indirectly on claim 1 and is therefore allowable over the primary reference Matsunaga for at least that reason. Moreover, none of the secondary references cited in combination with Matsunaga remedies the deficiencies in Matsunaga discussed above. Accordingly, the claims are allowable over the art of record. Withdrawal of the rejections is therefore respectfully requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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JAO:WEC/dxc
Date: July 18, 2007

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